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## **AC LINE FREQUENCY DIVIDERS**

## **RED SERIES**

RED 5/6 Divide by 5 or 6
RED 50/60 Divide by 50 or 60
RED 100/120 Divide by 100 or 120
RED 300/360 Divide by 300 or 360
RED 500/600 Divide by 500 or 600
RED 3000/3600 Divide by 3000 or 3600

## **FEATURES:**

- Clock input pulse shaper accepts 50Hz/60Hz sine wave directly
- Fully static counter operation
- +4.5V to +15V operation (VDD Vss)
- Low power dissipation
- High noise immunity
- Reset
- Input Enable
- 50Hz/60Hz division select input
- Output low power TTL compatible at +4.5V operation
- Square Wave Output (except for ÷ 5)
- RED x/y (DIP); RED x/y-S (SOIC) See Figure 1

## APPLICATION:

Time base generator from either 50 Hz or 60 Hz line frequency to produce:

10 pulses per second	(RED 5/6)
1 pulse per second	(RED 50/60)
1 pulse per 2 seconds	(RED 100/120)
1 pulse per .1 minute	(RED 300/360)
1 pulse per 10 seconds	(RED 500/600)
1 pulse per minute	(RED 3000/3600)

## **DESCRIPTION OF OPERATION:**

The counter advances by one on each negative transition of the input clock pulse as long as the Enable signal is High and the Reset signal is Low. When the Enable signal is Low the input clock pulses will be inhibited and the counter will be held at the state it was in prior to bringing the Enable Low. A High Reset signal clears the counter to zero count.

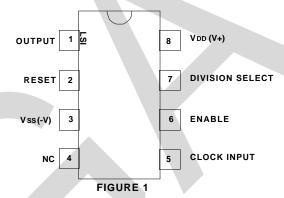
Depending on the device used, a Low on the Division Select input will cause a Divide by 6, 60, 120, 360, 600 or 3600. A High on the Division Select will cause a Divide by 5, 50, 100, 300, 500 or 3000.

All outputs are 50% duty cycle except RED 5, where output is low for two clocks and high for three clocks.

## **CLOCK INPUT**

If input signals are less than the Vss or greater than VDD, a series input resistor should be used to limit the maximum input current to 2 mA.

#### **PIN ASSIGNMENT - TOP VIEW**



# MARKING AS FOLLOWS: PART MARKING

RED 5/6	RED 6
RED 50/60	RED 60
RED 100/120	RED 120
RED 300/360	RED 360
RED 500/600	RED 600

#### **MAXIMUM RATINGS:**

RED 3000/3600

PARAMETER	SYMBOL	VALUE	UNIT
Storage Temperature	Tstg	-65 to +150	°C
Operating Temperatu	re Ta	-40 to +85	°C
DC Supply Voltage	(VDD - Vss)	+18	V
Voltage at any input	Vin	Vss - $0.3$ to VDD + $0.3$	V

**RED 3600** 

## **ENABLE SIGNAL TIMING**

If the Enable signal switches Low during a positive clock phase and then switches High during a negative clock phase, a false count will be registered. To prevent this from happening, the Enable signal should not switch Low during a positive clock phase unless the switch to High also occurs during a positive clock phase. The Enable signal should normally be switched during a negative clock phase.

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

- (	TA = 25° u	nless d	therwise s <sub>l</sub>	pecified)	Clock Rise and Fall Time:	<b>V</b> DD 5V		MAX num Limit	UNITS -
EST CONDITIONS: Vss = OV					–	10V		num Limit	-
Output Capa	acitance	Load	= 15 pF		Clock Frequency	5V	DC	600	KHz
Input Rise a except clock	and Fall t	imes :	= 20 ns,			10V	DC	1200	KHz
nput Capacitance = 5pF max (ar	ny input)				Input Clock Pulse Width	5V	800	-	ns
Quiescent Device Current	<b>V</b> dd 5V	Min -	<b>Max</b> 10	<b>Units</b> uA		10V	400	-	ns
	10V	-	20	uA	Output Rise and Fall Time	5V	-	225	ns
utput Voltage, Low Level	5V 10V	-	0.0	V V		10V	-	150	ns
High Level	5V	4.99	-	V	Propagation Delay to Output	5V	-	1500	ns
lock Input Voltage, Low Level	10V 5V	9.99	- 1	V V		10V	-	750	ns
-	10V	-	2	V	Enable Set-up Time	5V		300	ns
High Level	5V 10V	4 8	-	V V		10V		150	ns
nput Noise Immunity (except clock)	5V	1.5	-	V	Reset Pulse Width	5V	800		ns
(Low and High) Output Drive Current	10V	3.0	-	V		10V	400		ns
II 🖟 N Channel Sink Current	4.5V	0.18	-	mA	Reset Removal Time	5V		1200	ns
emp. (Vout = Vss +0.4V)	10V	0.45	-	mA	Neset Nemoval Hille	10V		600	ns
ange P Channel Sink Current	4.5V	0.3	-	mA	Donot Droma matter, D. I.	<b>5</b> ) (		1.400	m-
(Vout = VDD - 1)	10V	0.75	-	mA	Reset Propagation Delay to Output	5V 10V		1400 700	ns ns
					$\frac{\text{GND} - 3}{\text{N/C} - 4}$	– VSS			
_									
RED 5/6,50/60, 300/360,3000/3600							1	D5/6	
							1	]	
300/360,3000/3600							1	D5/6	
300/360,3000/3600 DS  CL 3 BIT	CL1_	3 BIT			BIT CL3 5 BIT		1	]	
300/360,3000/3600  DS  CL 3 BIT JOHNSON 15/4	CL1	3 BIT JOHNS ÷10		→ 3	BIT OHNSON +6 CL3 5 BIT JOHNSON +10		1	]	00
300/360,3000/3600 DS  CL  3 BIT JOHNSON		JOHNS		3	OHNSON CL3 JOHNSON			D50/60	00
300/360,3000/3600 DS  CL  3 BIT JOHNSON +5/6		JOHNS		3	OHNSON CL3 JOHNSON			D50/60	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6		JOHNS		3	OHNSON CL3 JOHNSON			D50/60	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120		JOHNS		3	OHNSON CL3 JOHNSON			D50/60 D3000/360	00
300/360,3000/3600 DS  CL  3 BIT JOHNSON +5/6		JOHNS		3	OHNSON CL3 JOHNSON			D50/60	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120	CL1	JOHNS ÷10	0	CL2	OHNSON CL3 JOHNSON +10			D50/60 D3000/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120  DS	CL1	JOHNS ÷10	T NSON	CL2	OHNSON CL3 JOHNSON			D50/60 D3000/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120  DS  CL  3 BIT JOHNSON	CL1	JOHNS ÷10	T NSON	CL2 1	DOHNSON ÷10  BIT			D50/60  D3000/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120  DS  CL  3 BIT JOHNSON	CL1	JOHNS ÷10	T NSON	CL2 1	DOHNSON ÷10  BIT			D50/60  D3000/360	90
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120  DS  CL  3 BIT JOHNSON	CL1	JOHNS ÷10	T NSON	CL2 1	DOHNSON ÷10  BIT			D50/60  D3000/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  RED 100/120  DS  CL  3 BIT JOHNSON +5/6	CL1	JOHNS ÷10	T NSON	CL2 1	DOHNSON ÷10  BIT			D50/60  D3000/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120  DS  CL  3 BIT JOHNSON +5/6	CL1	JOHNS ÷10	T NSON	CL2 1	DOHNSON ÷10  BIT			D50/60  D3000/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120  DS  CL  3 BIT JOHNSON +5/6  R  RED 500/600  DS	CL1	5 BI JOHNS +1(	T NSON 0	CL2 1 CL2 5	BIT +2			D50/60  D3000/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 500/600  DS  CL  3 BIT JOHNSON +5/6  R  RED 500/600  DS	CL1 CL1	5 BI JOHNS 5 BI JOHNS 5 BI JOHNS	T NSON O	CL2 1 CL2 5 5 JC	BIT +2			D50/60  D3000/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120  DS  CL  3 BIT JOHNSON +5/6  CL  3 BIT JOHNSON TOL  CL  3 BIT JOHNSON	CL1 CL1	5 Bi Johns +11	T NSON O	CL2 1 CL2 5 5 JC	BIT +2			D50/60  D3000/360  D300/360	00
300/360,3000/3600  DS  CL  3 BIT JOHNSON +5/6  R  RED 100/120  DS  CL  3 BIT JOHNSON +5/6  R  RED 500/600  DS	CL1 CL1	5 BI JOHNS 5 BI JOHNS 5 BI JOHNS	T NSON O	CL2 1 CL2 5 5 JC	BIT +2			D50/60  D3000/360  D300/360	90